I claim:

1. A memory cell array, comprising:

a semiconductor body having a doped well of a first conductivity typed formed therein and a top side;

a matrix-shaped configuration of memory transistors, each of said memory transistors having, at said top side of said semiconductor body, source/drain regions, a channel region disposed between said source/drain regions, a gate dielectric with a storage layer, and a gate electrode isolated from said channel region by said gate dielectric;

word lines disposed parallel to and at a distance from one another and having a row-wise connection to said gate electrodes;

bit lines disposed parallel to and at a distance from one another and having a column-wise connection to said source/drain regions, said bit lines being applied as strips of a semiconductor material doped for a second conductivity type being opposite said first conductivity type, on said top side of said semiconductor such that said source/drain regions being connected to one another column-wise; and

a barrier layer disposed as a diffusion barrier between said top side of said semiconductor body and said bit lines.

2. The memory cell array according to claim 1, wherein said bit lines are formed of an n-conductively doped polysilicon.

3. The memory cell array according to claim 1, wherein said barrier layer is formed of a silicon oxide of at least one atomic layer.

4. The memory cell array according to claim 1, wherein said barrier layer is formed of a silicon nitride of at least one atomic layer.

5. The memory cell array according to claim 1, wherein said barrier layer is formed of Al_2O_3 of at least one atomic layer.

6. The memory cell array according to claim 1, wherein said storage layer is provided for programming by charge trapping.

7. The memory cell array according to claim 1, wherein said semiconductor body has trenches formed therein, said gate electrodes are each disposed in one of said trenches between said source/drain regions, and said storage layer is present at least between a respective one of said gate electrodes and said source/drain regions.